

<b>Notice of References Cited</b>	Application/Control No.	Applicant(s)/Patent Under Reexamination	
	09/754,811	LIU ET AL.	
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**U.S. PATENT DOCUMENTS**

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	U	Liu et al, "BSIM3v3.2.2 MOSFET Model Users' Manual", The Regents University of California, 1999, pages 3-12: 3-13, 4-10:4-14
	V	Cheng et al, "A Physical and Scalable I-V Model in BSIM3v3 for Analog/Digital Circuit Simulation", IEEE Transactions on Electron Devices, Vol. 44, No. 2, February 1997
	W	Park et al, "A Charge Sheet Capacitance Model of Short Channel MOSFET's for SPICE", IEEE Transactions on Computer-Aided Design, Vol. 10, No. 3, March 1991
	X	Barby et al, "Polynomial Splines for MOSFET Model Approximation", IEEE Transactions on Computer-Aided Design, Vol. 7, No. 3, May 1988

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

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	U	Liu, William, "MOSFET Models for SPICE Simulation Including BSIM3v3 and BSIM4", John Wiley & Sons, Inc. 2001, pages 27-30.
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